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LETTER TO THE EDITOR

High aspect ratio piezoelectric strontium–bismuth–tantalate nanotubes

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Abstract

We report the deposition and characterization of transparent ferroelectric/piezoelectric nanotubes of wall thickness about 40 nm, tube diameters ranging from a few hundred nanometres to 4 μm, and length about 100 μm. Comparison with other nanotubes is made and applications in dynamic random access memory trenching and ink-jet printers are discussed.

1. Introduction

Nanotubes of conducting materials such as carbon have recently received considerable attention. Microtubes of nonconducting BN and SiC have also been reported in the literature [1–3][1]. However, ferroelectric nanotubes made of oxide insulators, as reported here, have a variety of applications in pyroelectric detectors, piezoelectric ink-jet printers, and memory capacitors that cannot be filled by other nanotubes [4–8]. In the drive for increased storage density in FRAM and dynamic random access memory (DRAM) devices, complicated stacking geometries, 3D structures, and trenches with high aspect ratios are also being investigated with a view to increasing the dielectric surface area. The integration of ferroelectric nanotubes into Si substrates, shown here, is particularly important in construction of 3D memory devices beyond the present stacking and trenching designs, which according to the international ULSI schedule [9] must be achieved by 2008.

Template synthesis of nanotubes and wires is a versatile and inexpensive technique for producing nanostructures. The size, shape, and structural properties of the assembly are simply controlled by the template used. Using carbon nanotubes as templates, tubular forms of a number of oxides including V_2O_5, SiO_2, Al_2O_3, and ZrO_2 have been generated [10]. Much larger (>20 μm diameter) ferroelectric microtubes have been made by sputter deposition around polyester fibres [3, 11]—Fox has made them from ZnO and $PbZr_{1-x}Ti_xO_3$ (PZT), with 23 μm inside diameter, about 1000 times larger than the smallest nanotubes reported in the present paper.

Porous sacrificial templates as opposed to fibres have also been used. Porous anodic alumina has a polycrystalline structure with ordered domains of diameter 1–3 μm, containing

[1] [3] claims piezoelectric nanotubes of boron nitride deposited on top of SiC cores.

self-organized 2D hexagonal tubular pore arrays with an interpore distance of 50–420 nm [12]. This nanochannel material can therefore be used as a template for individual nanotubes, but is not suitable for making an ordered array of tubes over length scales greater than a few micrometres. Many oxide nanotubes, such as TiO_2, In_2O_3, Ga_2O_3, $BaTiO_3$, and $PbTiO_3$, as well as nanorods of MnO_2, Co_3O_4, and TiO_2, have been made using porous alumina membranes as templates [10].

Hernandez *et al* [13] used a sol–gel template synthesis route to prepare $BaTiO_3$ and $PbTiO_3$ nanotube bundles by dipping alumina membranes with 200 nm pores into the appropriate sol. The $BaTiO_3$ and $PbTiO_3$ nanotubes were shown to be cubic (paraelectric) and tetragonal (ferroelectric), respectively, by means of x-ray diffraction, although Raman studies indicated some non-centrosymmetric phase on a local scale in the $BaTiO_3$.

Porous silicon materials are also available as suitable templates. Mishina *et al* [14, 15] used a sol–gel dipping technique to fill nanoporous silicon with a PZT sol producing nanograins and nanorods 10–20 nm in diameter. The presence of the ferroelectric PZT phase was shown by second harmonic generation (SHG) measurements. In this instance the porous silicon does not have a periodic array of pores [16] and, as in the case for those produced by Hernandez *et al*, we emphasize that those nanotubes are not ordered arrays, but instead spaghetti-like tangles of nanotubes that cannot be used for the Si device embodiments.

Porous Si templates of a second type, however, consist of a very regular periodic array of pores with very high aspect ratios. By a combination of photolithography and electrochemical etching, hexagonal or orthogonal arrays of pores with diameters 400 nm to a few micrometres and up to 100 μm deep can be formed in single crystal Si wafers [17, 18]. These crystals were originally developed for application as 2D photonic crystals, but also find applications as substrates for templated growth and integration of oxide nanostructures with Si technology. Alexe *et al* [19] recently used such crystals to produce individual, free standing PZT and $BaTiO_3$ ferroelectric nanotubes by a polymeric wetting technique. In previous work, we described the use of liquid source misted chemical deposition (LSMCD) [20, 21] to fill such photonic Si crystals with $SrBi_2Ta_2O_9$ (SBT) precursor [22]. During deposition, the SBT precursor was shown to coat the inside of the pores [22]. In this study we report the use of LSMCD to produce high aspect ratio ferroelectric nanotubes of SBT both embedded in Si for memory applications and also as a discrete, regular array of nanotubes. A number of possible applications are also discussed.

2. Experimental details

Porous Si substrate with a regular hexagonal array of pores with diameters about 2 μm and 800 nm and depth 100 μm were exposed to repeated misted deposition of the liquid precursor using Samco MD-6060 apparatus. A flat SBT film was also deposited on a $Pt/Ti/SiO_2/Si$ substrate using the same deposition conditions. The chemical precursor solution consisted of a 0.1 M solution of Sr, Bi, Ta ethylhexanoates in toluene (Epichem, Mildenhall, UK), with appropriate ratios of Sr, Bi, and Ta to give the resulting stoichiometry $Sr_{0.8}Bi_{2.2}Ta_2O_9$ [22]. All substrates underwent repeated depositions with a two step pyrolysis between consecutive stages: the filled porous substrates were pyrolysed for 30 min at 100 °C and then 30 min at 300 °C, while the SBT film was pyrolysed for 1 min at 100 °C and 5 min at 300 °C. After final deposition and pyrolysis, the filled photonic substrates and SBT film were thermally annealed at 850 °C for 30 min in air. The degree of crystallinity was determined by means of XRD (BEDE D1D1 diffractometer). Etching of the Si substrate was carried out in an aqueous HF/HNO_3 solution (15/50 vol%). Ferroelectric hysteresis loops were obtained at room temperature using a Radiant Technologies 'Precision Premier' tester. Au electrodes were sputtered through a shadow mask.

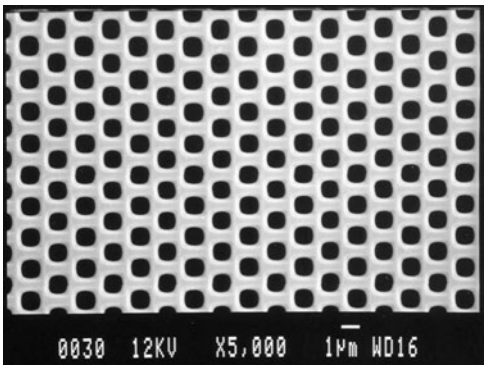

Figure 1. An SEM micrograph of porous, photonic Si crystals with a hexagonal array of pores with diameter 800 nm, depth about 100 μm.

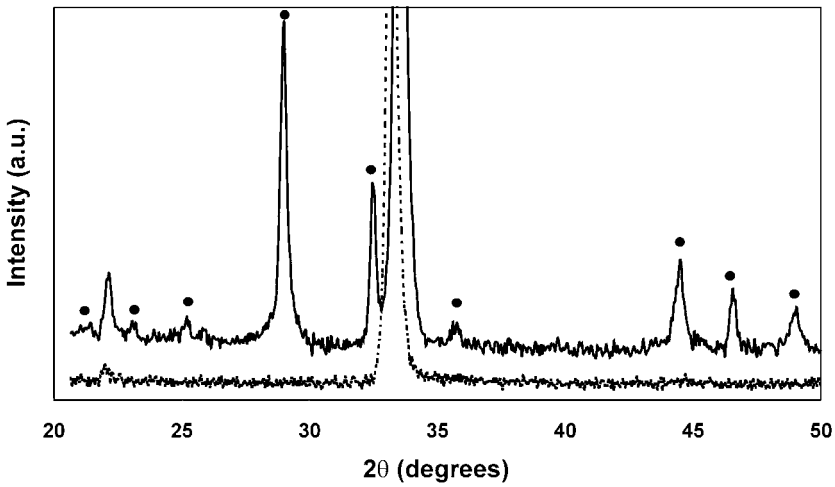

Figure 2. XRD by a photonic crystal with pore diameter 800 nm, before (- - - -) and after filling (—), indicating the presence of crystalline phase $Sr_{0.8}Bi_{2.2}Ta_2O_{9+\gamma}$ (•).

3. Results and discussion

An SEM micrograph of an unfilled photonic crystal with pore diameter about 800 nm is shown in figure 1. After repeated depositions and thermal annealing, XRD analysis of the porous photonic substrates revealed the presence of crystalline SBT. XRD data for the filled photonic crystal with pore diameter 800 nm are shown in figure 2. The most intense reflection at about 33°–34° 2θ and the weak reflection at 22° 2θ are due to the substrate, as indicated by the data obtained from the 'blank' photonic crystal before filling. The other reflections are consistent with crystalline SBT of stoichiometry $Sr_{0.8}Bi_{2.2}Ta_2O_{9+\gamma}$ [23]. The relative intensities do not indicate any epitaxy, suggesting the deposited SBT phase is a randomly orientated polycrystalline ceramic.

After etching of the photonic crystal with pore diameter 2 μm for 30 s with aqueous HF/HNO_3 the interface between the Si substrate and SBT coating is dissolved, exposing the uniform SBT tube; see figure 3(a). The tube walls are very uniform with a thickness of about 200 nm. The same sample is shown in cross-sectional view after complete removal of the host

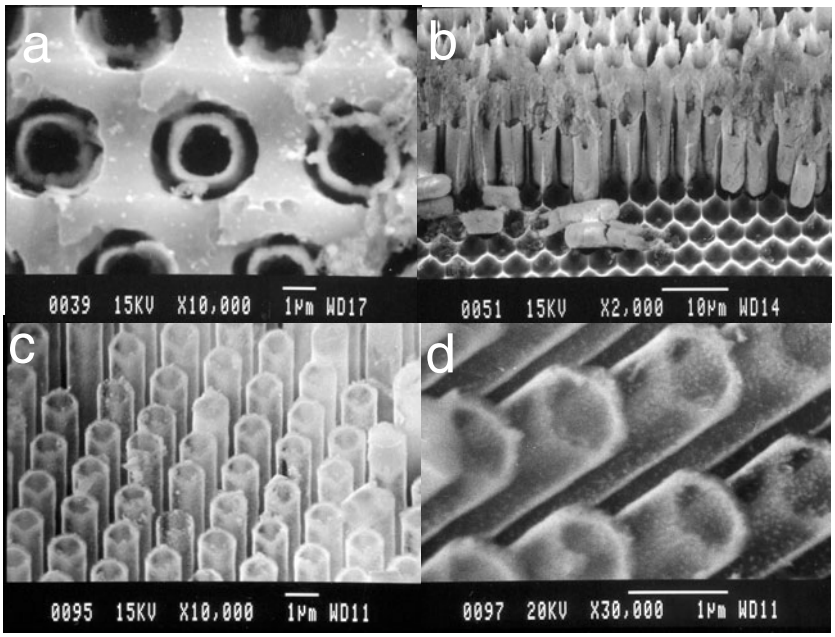

Figure 3. (a) An SEM micrograph indicating a plan view of a regular array of SBT tubes in the host silicon substrate with diameter about 2 μm and wall thickness about 200 nm. (b) SBT tubes in cross-sectional view indicating coating to the bottom of the pore. (c) A micrograph of a free standing array of tubes with diameter about 800 nm and (d) wall thickness $<$100 nm.

Si walls between pores; figure 3(b). The result is a regular array of tubes attached to the host Si matrix only at the tube base. Although these tubes have suffered damage during handling, it is clear that the pores have been filled uniformly to the bottom, at a depth of about 100 μm.

The second photonic crystal with pore diameter 800 nm underwent fewer depositions and after etching revealed a regular array of uniform tubes of diameter 800 nm; figure 3(c). The wall thickness is uniform and $<$100 nm; figure 3(d). The tubes are about 100 μm long, are completely discrete, and are still attached to the host Si matrix, creating a perfectly registered hexagonal array. Free standing tubes may be produced by completely dissolving the host Si matrix.

Although XRD indicates the presence of crystalline $Sr_{0.8}Bi_{2.2}Ta_2O_{9+\gamma}$ which should exhibit ferroelectricity, it was not possible to make electrical contact to the tubes to confirm this. The flat SBT film, however, was deposited and annealed under the same conditions and was used for comparison. XRD analysis of the film showed the presence of the same SBT phase; figure 4. Polarization–electric field measurements showed a classic hysteretic P–E loop associated with ferroelectricity; figure 5. The average coercive field, E_C (calculated from the average of forward, $+E_C$, and reverse, $-E_C$, switching fields), was 41.75 kV cm^{-1}. By inference, the SBT tubes grown under identical conditions should also exhibit ferroelectricity. This has significant implications for applications which would utilize both ferroelectric and piezoelectric properties.

As yet, we have not applied electrodes to the tubes; however, Steinhart *et al* [24] recently used porous anodic alumina templates to grow palladium nanotubes. Using a similar method we hope to alternately deposit Pd or Pt and SBT to produce a concentric electrode/FE/electrode structure in each nanotube. The use of the photonic crystal template with a regular array of pores has significant benefits over other porous substrates in that the coatings/tubes produced are

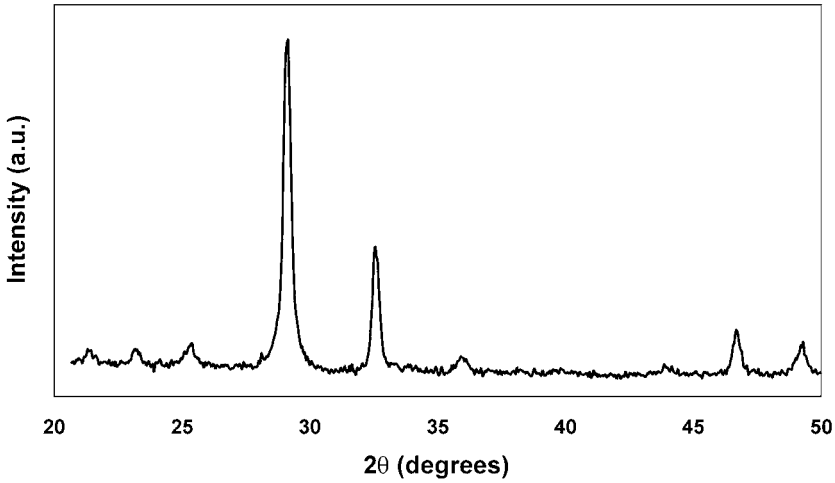

Figure 4. XRD by a flat SBT film on a Pt/Ti/SiO_2/Si substrate indicating the presence of crystalline phase $Sr_{0.8}Bi_{2.2}Ta_2O_{9+\gamma}$.

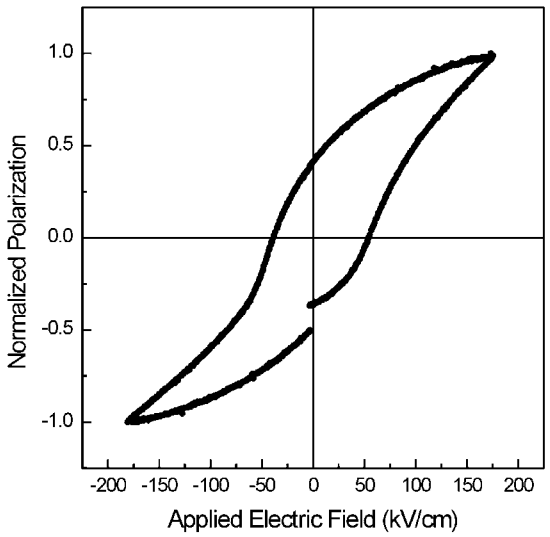

Figure 5. A P–E hysteresis loop of SBT film indicating ferroelectric switching.

also in a registered array ordered over several millimetres or even centimetres. This facilitates addressing of such an array for device applications.

DRAMs utilize high surface area dielectrics, and high aspect ratio SBT coatings such as these embedded in Si could increase storage density. Current state-of-the-art deep trenched capacitors are 0.1 μm diameter by 6 μm deep, aspect ratio 60:1. Using SBT (or other FE oxide) nanotubes of wall thickness $<$100 nm, a trench (or array of trenches) of 0.1 μm diameter and 100 μm deep, with an aspect ratio of $>$1000:1, is possible. Applying and addressing electrodes to an array of FE nanotubes could generate 3D FRAM structures offering high storage density with improved read/write characteristics compared to conventional planar stacks.

On removal of the Si walls, the piezoelectric response (expansion/contraction under an applied field) of such an array of nanotubes could be utilized for a number of MEMs

applications. These could include: (1) ink-jet printing—delivery of sub-picolitre droplets for lithography free printing of submicron circuits; (2) biomedical applications—nanosyringes, inert drug delivery implants; (3) micropositioners or movement sensors.

4. Conclusions

Using porous photonic Si crystals with a regular array of pores of diameter 400 nm to a few microns and 100 μm deep as templates, we have successfully produced uniform coatings of FE SBT $<$100 nm thick with high aspect ratios. These coatings have potential application in DRAM and FRAM devices. On partial removal of the Si template, it is possible to produce a periodic array of nanotubes in which each tube is completely discrete. This is in contrast to other template approaches, which produce either individual, free standing nanotubes or 'bundled' or entangled structures. The formation of a periodic array has several advantages in terms of addressing/registration for device applications.

Just as various applications of carbon nanotubes have been investigated, it is envisioned that oxide nanotubes can be used in fluidic devices for analysis and control of molecular species, nanoelectronic devices, catalysis, and nanoscale delivery vehicles. The very large surface/volume ratio makes catalytic devices particularly attractive. Piezoelectric and ferroelectric nanotubes of SBT therefore have potential for a variety of applications in addition to those in ferroelectric memory devices.

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